University of Southern California

ECE 105: Introduction to Electrical Engineering

Lecture 5

Device 1

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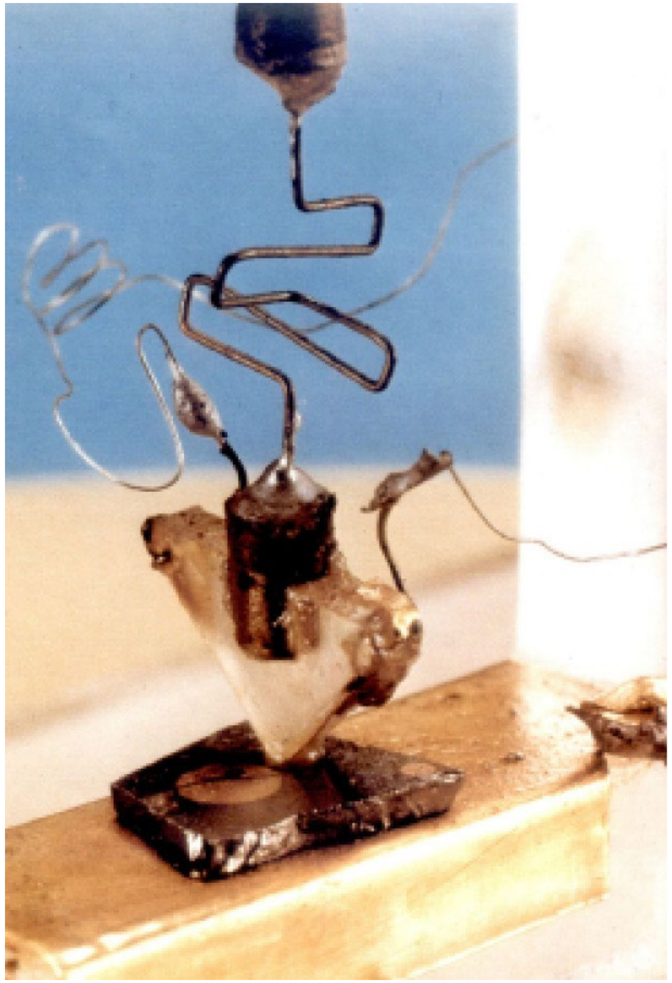
Rehan Kapadia

The First Transistor



1956 Physics Nobel Prize

"for their researches on semiconductors and their discovery of the transistor effect"

William Bradford Shockley

1/3 of the prize

USA

Semiconductor Laboratory of Beckman Instruments, Inc.
Mountain View, CA, USA

John Bardeen

1/3 of the prize

USA

University of Illinois
Urbana, IL, USA

Walter Houser Brattain

1/3 of the prize

USA

Bell Telephone Laboratories
Murray Hill, NJ, USA

Invention of the Field-Effect Transistor

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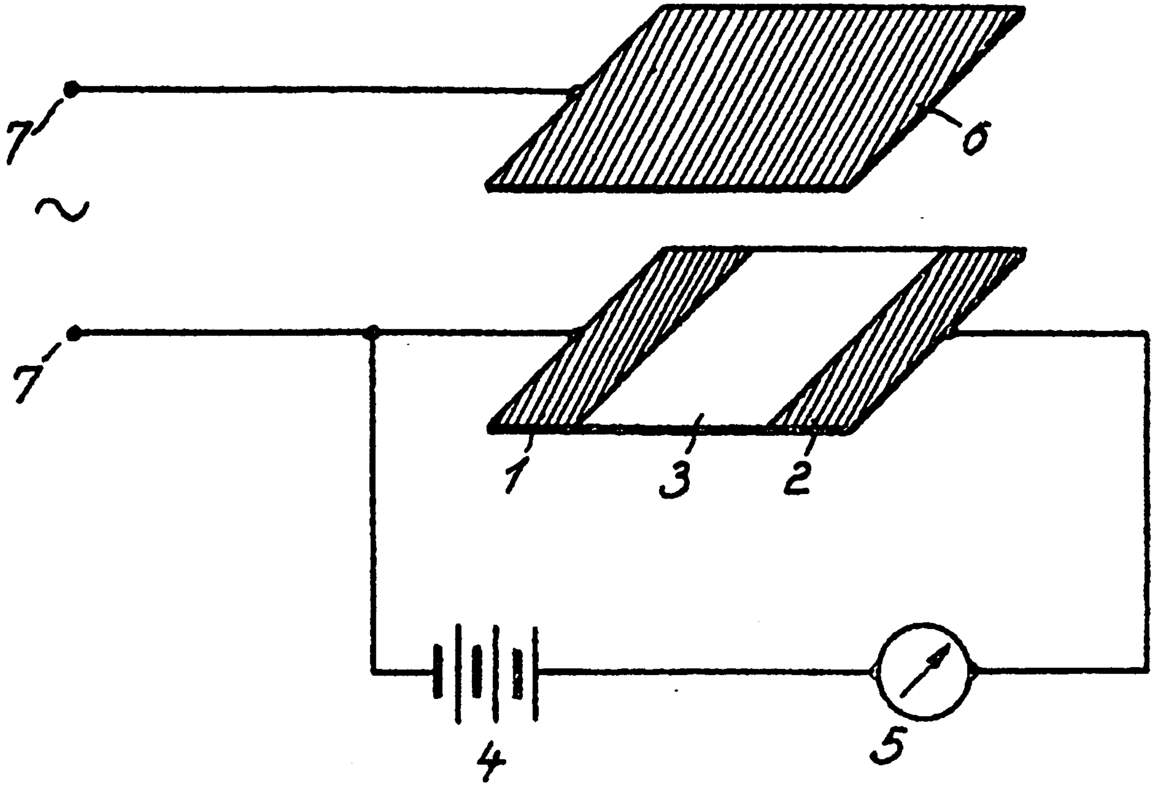


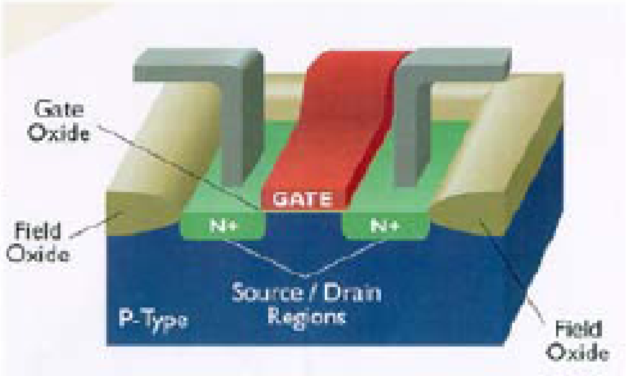
In 1935, a British patent was issued to Oskar Heil.
A working MOSFET was not demonstrated until 1955.

Modern Field Effect Transistor (FET)

- An electric field is applied normal to the surface of the semiconductor (by applying a voltage to an overlying electrode), to modulate the conductance of the semiconductor

→ Modulate drift current flowing between 2 contacts ("source" and "drain") by varying the voltage on the "gate" electrode

N-channel MOSFET:



Introduction to the MOSFET

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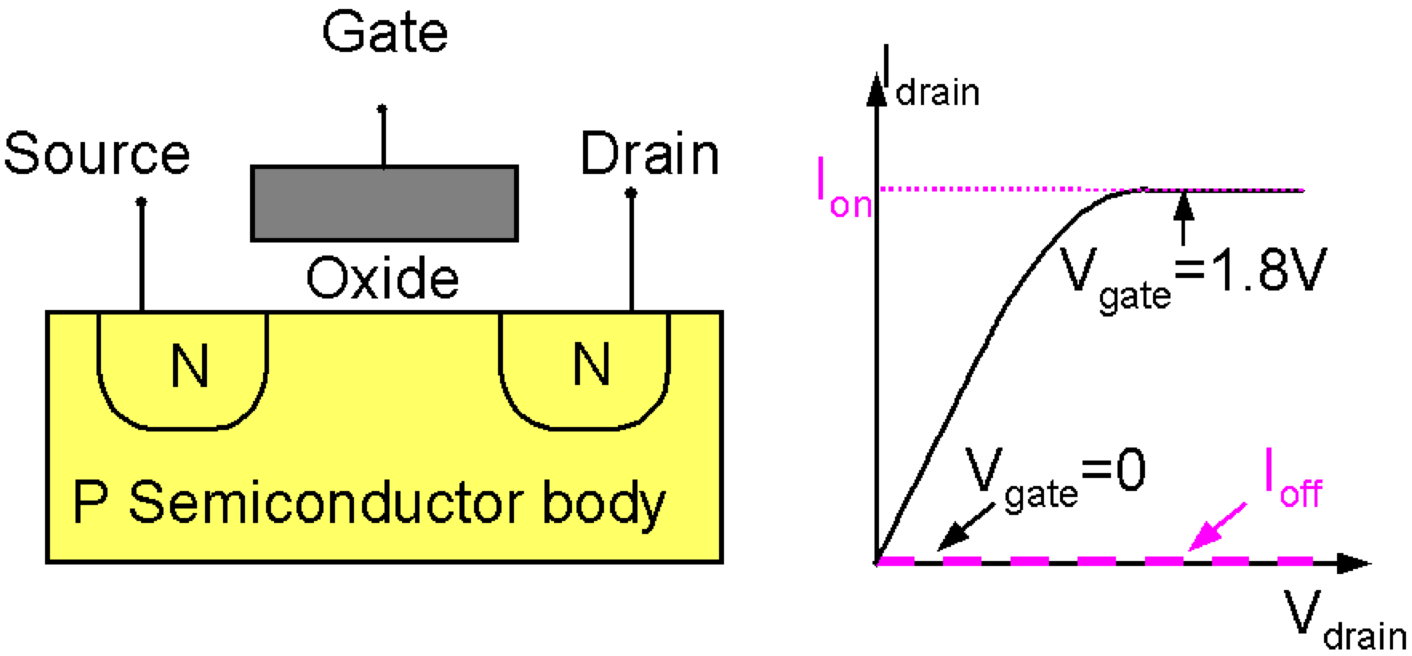
Basic MOSFET structure and IV characteristics

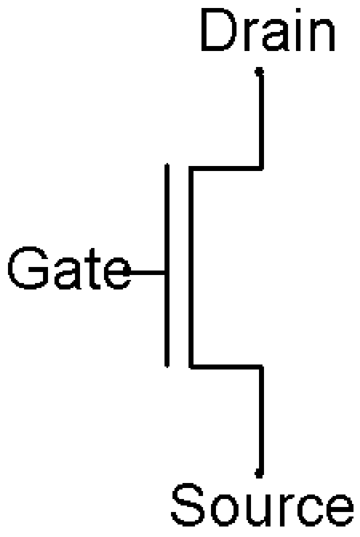


What is desirable: large I_{on}, small I_{off}

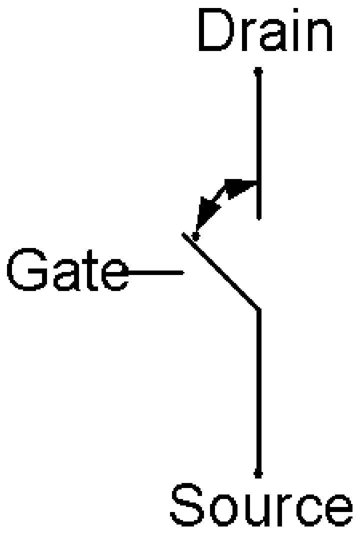
Introduction to the MOSFET

Two ways of representing a MOSFET:

Circuit Symbol

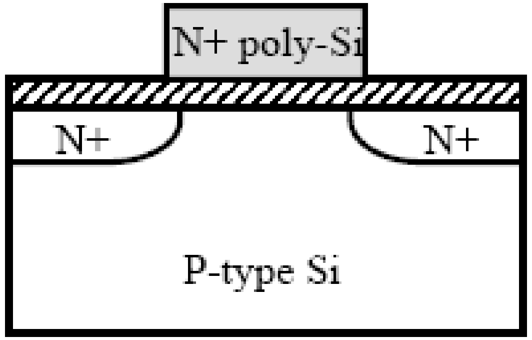


Simple Switch



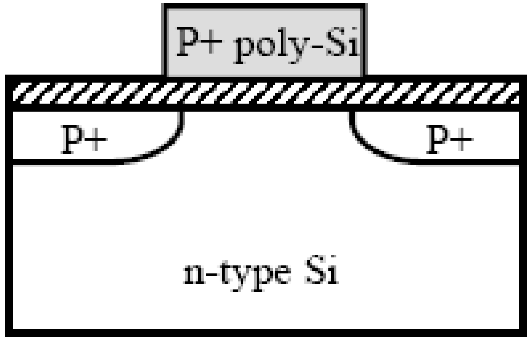
N-channel *vs.* P-channel

NMOS



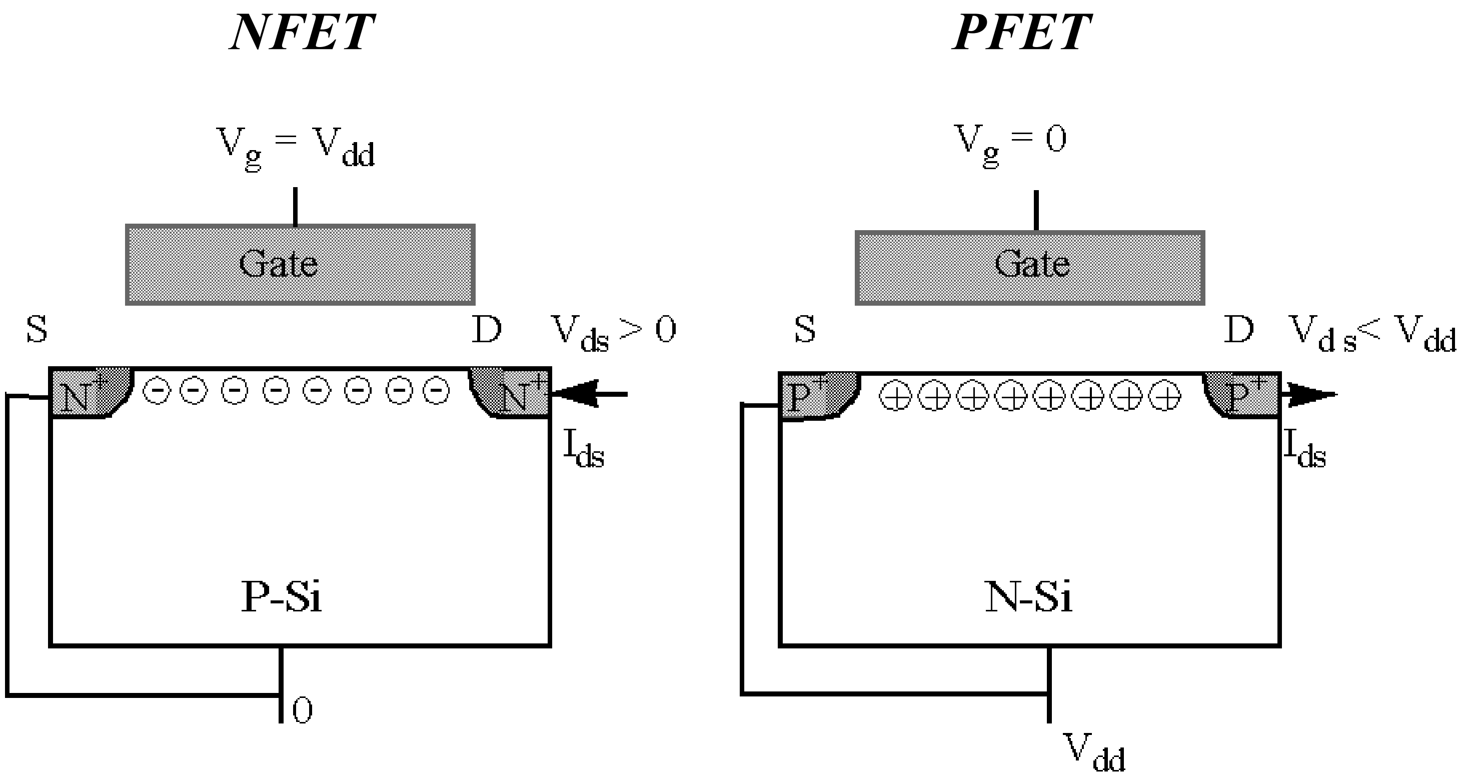
- For current to flow, $V_{GS} > V_T$
- Enhancement mode: $V_T > 0$
- Depletion mode: $V_T < 0$
  - Transistor is ON when V_G=0V

PMOS



- For current to flow, $V_{GS} < V_T$
- Enhancement mode: $V_T < 0$
- Depletion mode: $V_T > 0$
  - Transistor is ON when V_G=0V

Complementary MOSFETs (CMOS)



When $V_g = V_{dd}$, the NFET is on and the PFET is off.
When $V_g = 0$, the PFET is on and the NFET is off.

CMOS (Complementary MOS) Inverter

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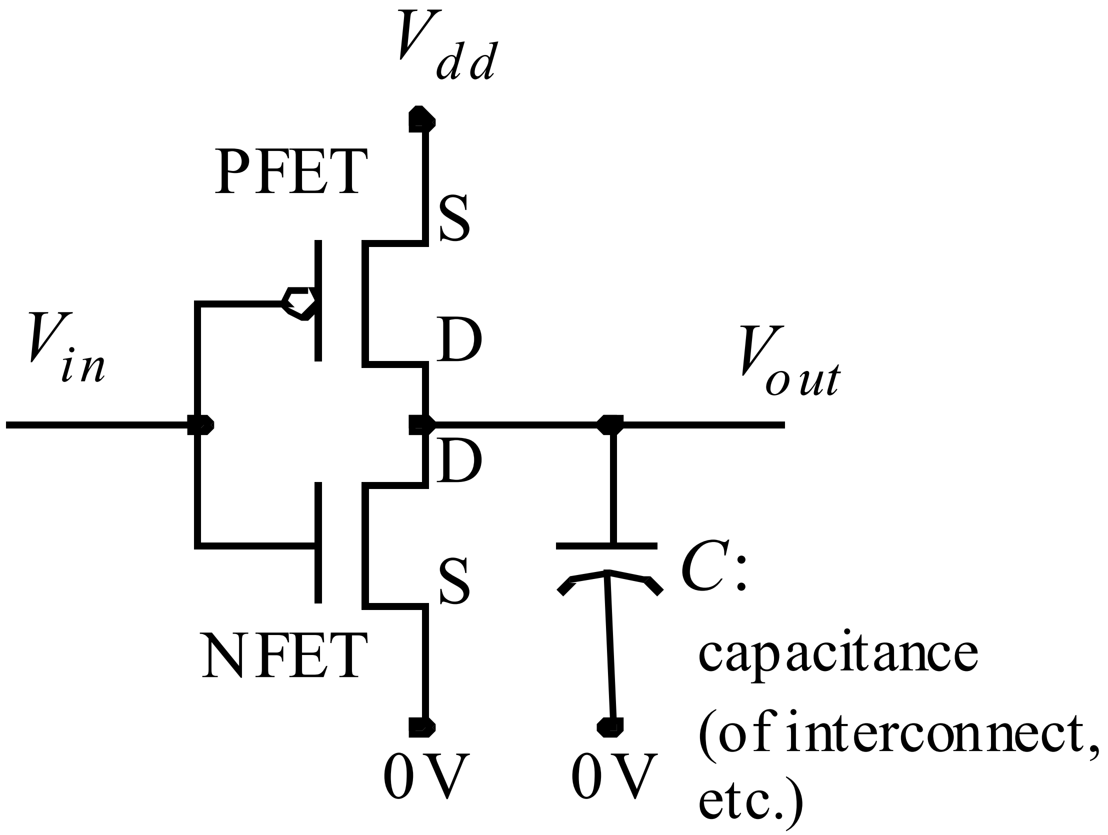

Qualitative discussion: n-MOSFET

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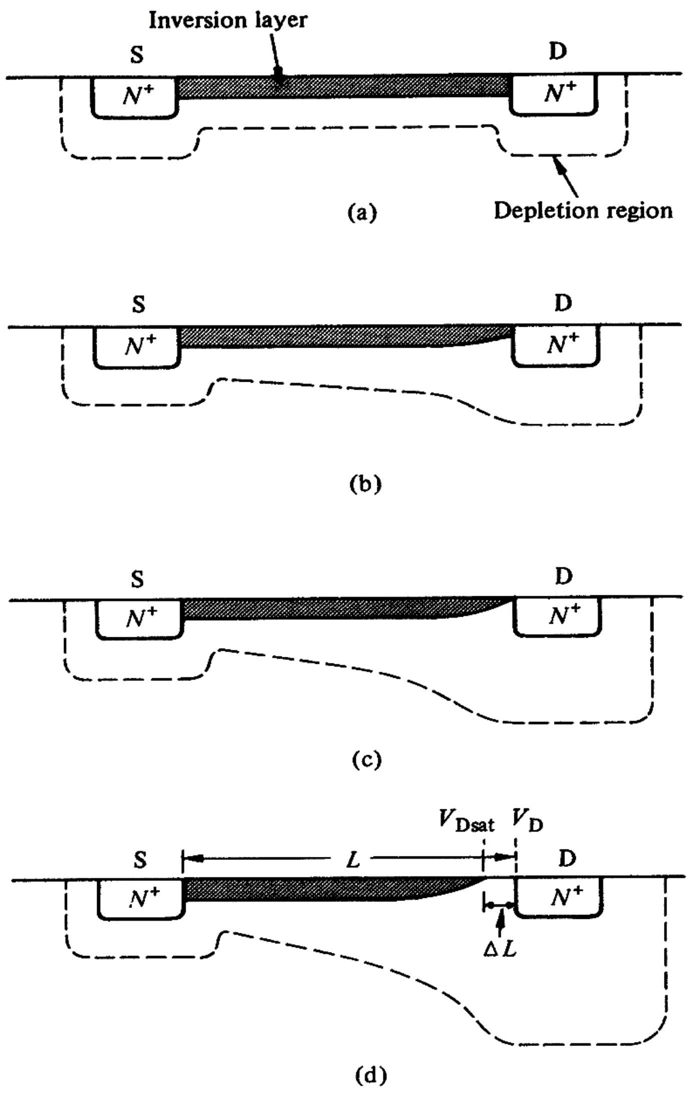


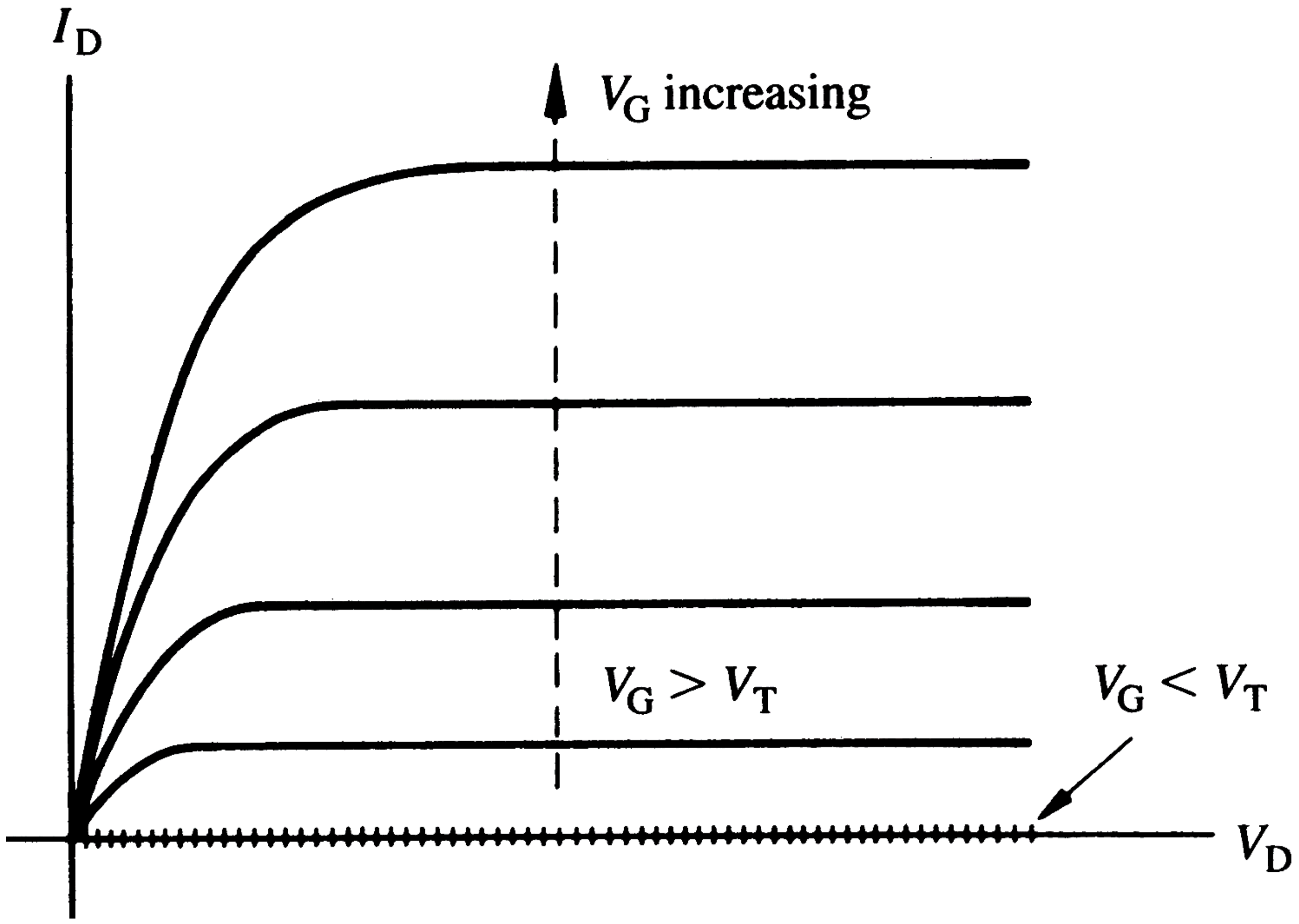
$V_G > V_T$; $V_{DS} \approx 0$
I_D increases with V_{DS}

$V_G > V_T$; V_{DS} small, > 0
I_D increases with V_{DS} , but rate of increase decreases.

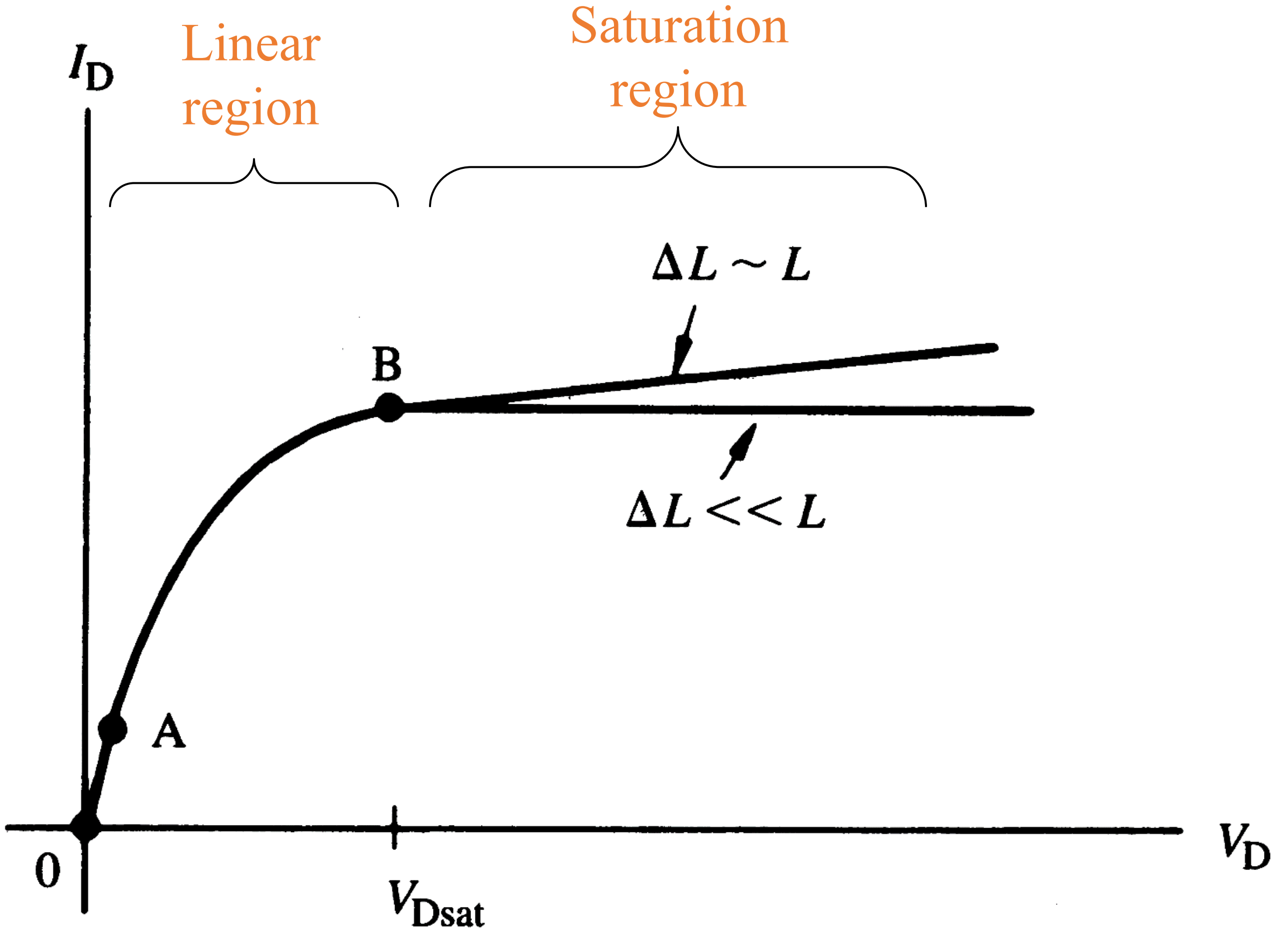
$V_G > V_T$; $V_{DS} \approx$ pinch-off
I_D reaches a saturation value, $I_{D,sat}$
The V_{DS} value is called $V_{DS,sat}$

$V_G > V_T$; $V_{DS} > V_{DS,sat}$
I_D does not increase further, saturation region.

I_D-V_{DS} characteristics expected from a long channel ($\Delta L << L$) MOSFET (n-channel), for various values of V_G



I_D-V_{DS} characteristics for n-MOSFET



Quantitative I_D-V_{DS} Relationships – 1st attempt "Square Law"

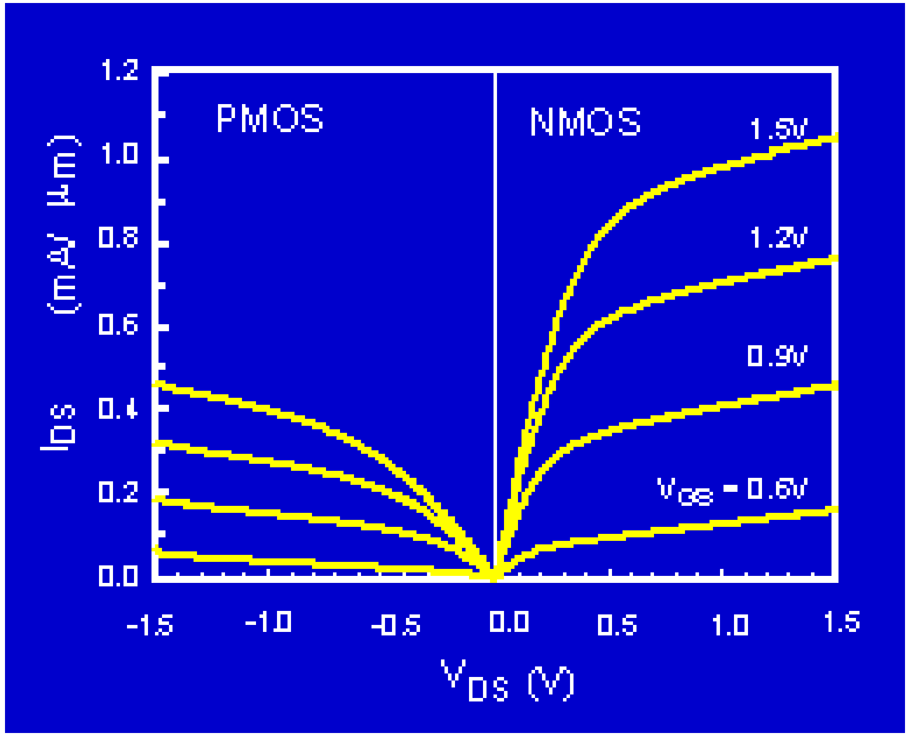
$$I_D = \frac{Z\mu_n}{L} C_{ox} \left[(V_G - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad 0 < V_{DS} < V_{DS,sat} \quad ; \quad V_G > V_T$$

I_D will increase as V_{DS} is increased, but when $V_G - V_{DS} = V_T$, pinch-off occurs, and current saturates when V_{DS} is increased further. This value of V_{DS} is called $V_{DS,sat}$. i.e., $V_{DS,sat} = V_G - V_T$ and the current when $V_{DS} = V_{DS,sat}$ is called $I_{DS,sat}$.

$$I_{D,sat} = \frac{Z \mu C_{ox}}{2L} (V_G - V_T)^2 \qquad V_D > V_{DS,sat} \quad ; \quad V_G > V_T$$

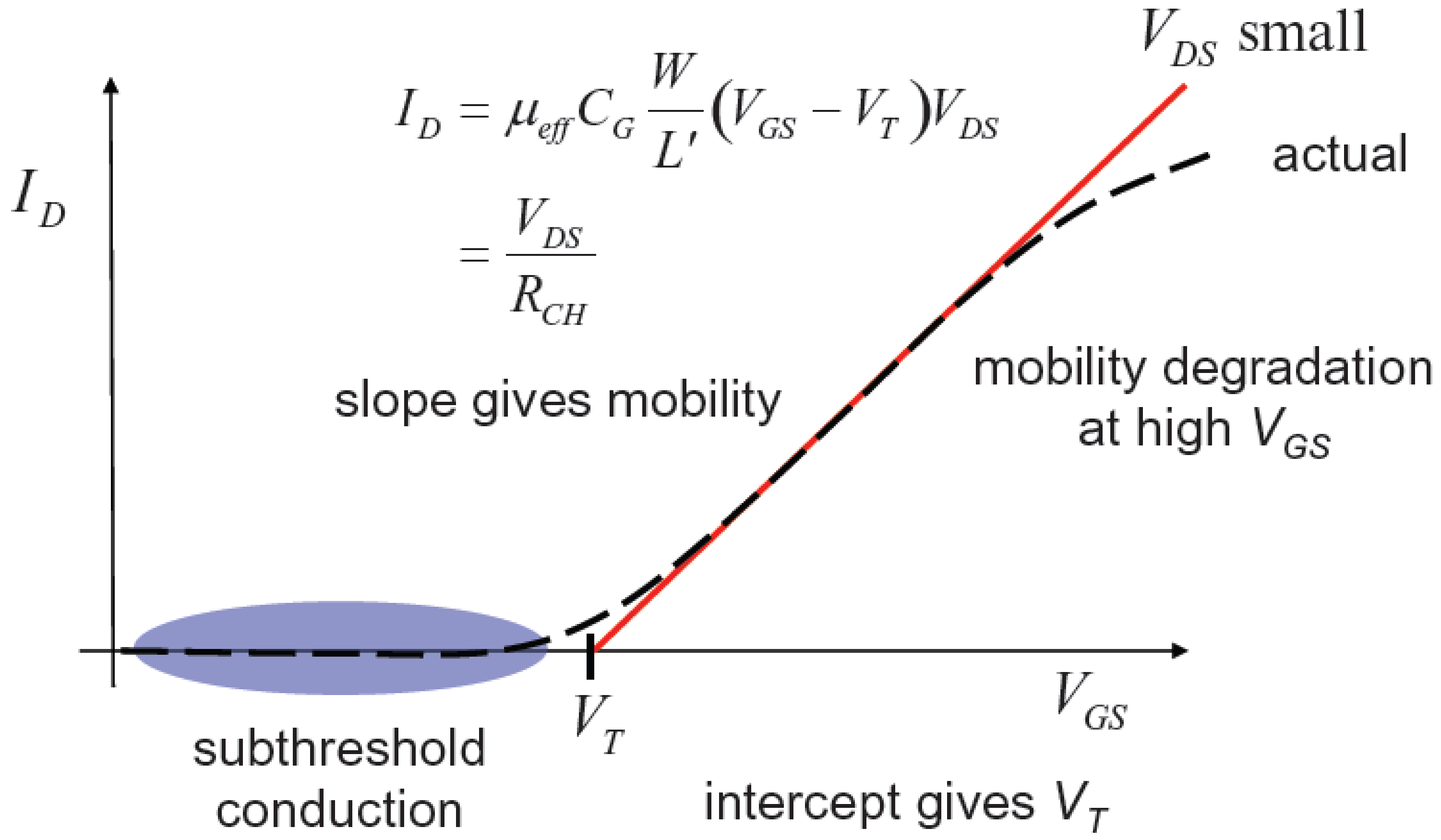
Here, C_{ox} is the oxide capacitance per unit area, $C_{ox} = \varepsilon_{ox} / x_{ox}$

P-MOSFET N-MOSFET IV Characteristics



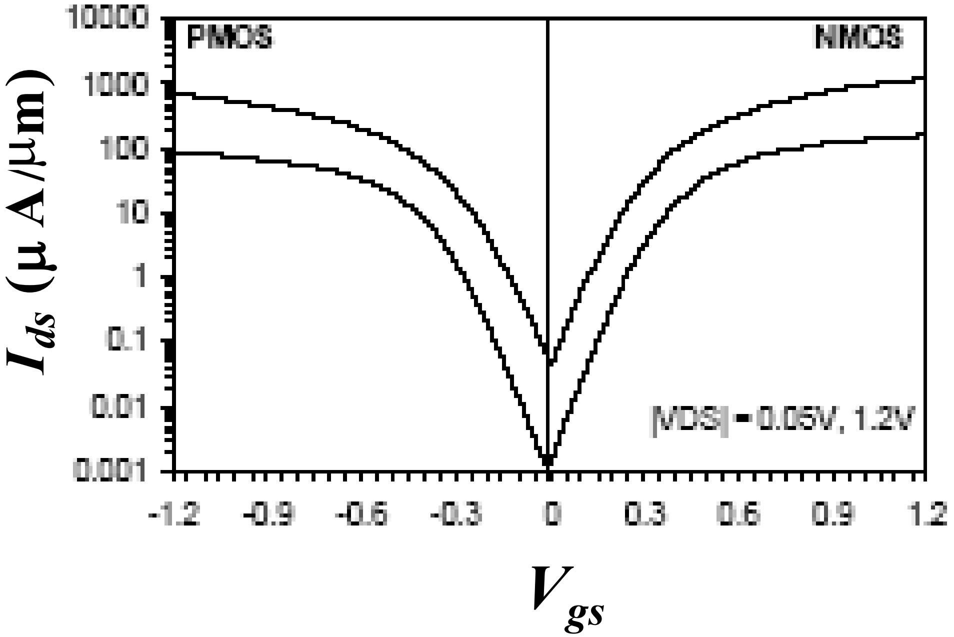
The PMOS IV is qualitatively similar to the NMOS IV, but the current is about half as large. Why?

Threshold and Subthreshold



Subthreshold Current

- The leakage current that flows at $V_g < V_t$ is called the subthreshold current. Previously we had assumed that current is zero, but in reality that's not the case.



Intel, T. Ghani et al., IEDM 2003

90nm technology. Gate length: 45nm for NMOS, 50nm for PMOS

- The current at $V_{gs}=0$ and $V_{ds}=V_{dd}$ is called I_{off}.