Practice Midterm A SOLUTIONS

Modules 1 and 2 · Lectures 5 to 7, 9 and 10

Instructions

- Time: 120 minutes. Total: 100 points.
- Part I has 8 short problems (50 points). Plan about 45 minutes for Part I.
- Part II has 4 long problems (50 points). Plan about 65 minutes for Part II. Keep about 10 minutes to check your answers.
- Do not use a calculator. The numbers in each problem need only simple mental arithmetic.
- Show your method for each answer. Give the unit with each numerical answer.
- Where a problem tells you to leave an expression in a given form, do not reduce it further. You can leave a result such as 4/3 mA as a fraction.
- All wires and sources are ideal, unless a problem gives other data.
- Power: an element absorbs $P = V \cdot I$ when its current enters its "+" terminal (passive sign convention). When the current leaves the "+" terminal, the element supplies $P = V \cdot I$.
- Notation: V_T is the MOSFET threshold voltage. kT/q is the thermal voltage in the diode equation. V_{TH} is a Thevenin voltage. I_s is the reverse saturation current of a diode.
- With resistances in kΩ and voltages in V, currents come out in mA and powers in mW.

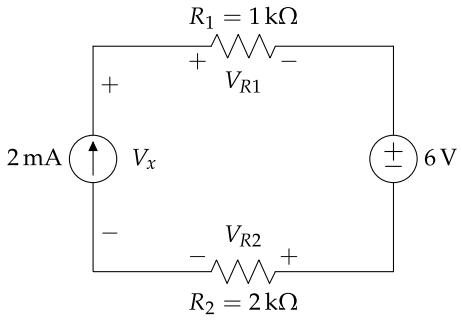
Constants

- $q = 1.602 \times 10^{-19}$ C. Use $q \approx 1.6 \times 10^{-19}$ C in hand calculations.
- $n_i = 10^{10}$ cm^{-3} for Si at 300 K, and $n \cdot p = n_i^2$.
- $kT/q = 0.026$ V at 300 K.
- $\ln 10 \approx 2.3$, so $(kT/q) \cdot \ln 10 \approx 0.06$ V.
- Photon energy: $E\ (\text{eV}) = 1240 / \lambda\ (\text{nm})$.
- Band gaps (L9-16): Ge 0.67 eV, Si 1.12 eV, GaAs 1.42 eV, GaP 2.25 eV, diamond 6.0 eV.
- Lengths: 1 cm = 10 mm = 10^4 μm.
- Prefixes: f = 10^{-15}, n = 10^{-9}, μ = 10^{-6}, m = 10^{-3}, k = 10^3, M = 10^6.

Part I · Short problems (50 points)

Problem 1 CIRCUITS EASY 6 POINTS

A 2 mA current source, two resistors and a 6 V source form one loop. The figure shows the polarities of V_x, V_{R1} and V_{R2}.



(a) Find the current in R_1 and in R_2. Find V_{R1} and V_{R2}. (2 points)

(b) Use KVL to find the voltage V_x across the current source. (2 points)

(c) Find the power of each source. State whether each source absorbs or supplies power. (2 points)

SOLUTION

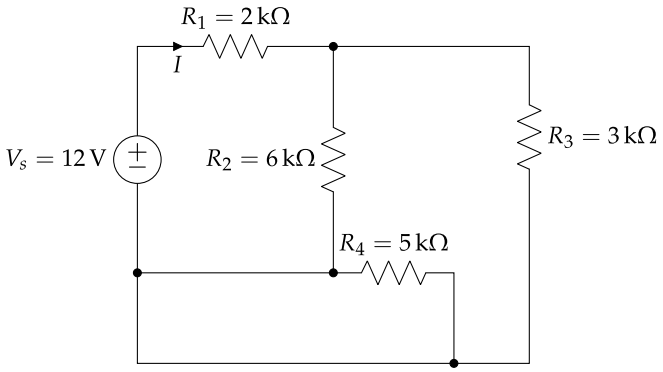
(a) The four elements form one loop, and each node joins only two elements. So KCL gives the same current in all four elements. The current source fixes this current (L5-8): **2 mA, clockwise, in R_1 and in R_2**. Ohm's law gives $\mathbf{V_{R1} = 2\ mA \times 1\ k\Omega = 2\ V}$ and $\mathbf{V_{R2} = 2\ mA \times 2\ k\Omega = 4\ V}$. The current enters the "+" end of each resistor, as the figure shows.

(b) Go clockwise around the loop from the bottom-left corner (L5-10). The potential rises by V_x through the current source. It drops by 2 V across R_1, by 6 V through the 6 V source (from "+" to "−"), and by 4 V across R_2. So $V_x - 2\ V - 6\ V - 4\ V = 0$, and $\mathbf{V_x = 12\ V}$. The rest of the circuit sets this voltage; the current source does not fix it (L5-8).

(c) The current leaves the "+" terminal of the current source, so the **current source supplies 12 V × 2 mA = 24 mW**. The current enters the "+" terminal of the 6 V source, so the **6 V source absorbs 6 V × 2 mA = 12 mW**, like a battery under charge (passive sign convention, L6-17). Check: the resistors absorb 2 V × 2 mA + 4 V × 2 mA = 12 mW, and 12 mW + 12 mW = 24 mW, which equals the power supplied.

Problem 2 CIRCUITS EASY 6 POINTS

The circuit has one source and four resistors.



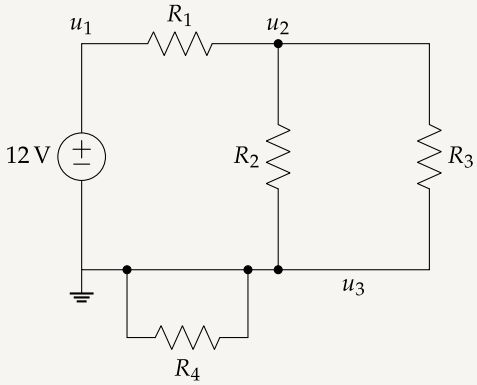
(a) How many distinct nodes does the circuit have? (Wires that connect form one node.) (2 points)

(b) One resistor carries no current. Name it and explain why. (1 point)

(c) Find the equivalent resistance R_{eq} that the source sees and the source current I. Then use the current divider to find the current in R_3. (3 points)

SOLUTION

The redrawn circuit shows the three nodes. R_4 has both ends on node u_3.



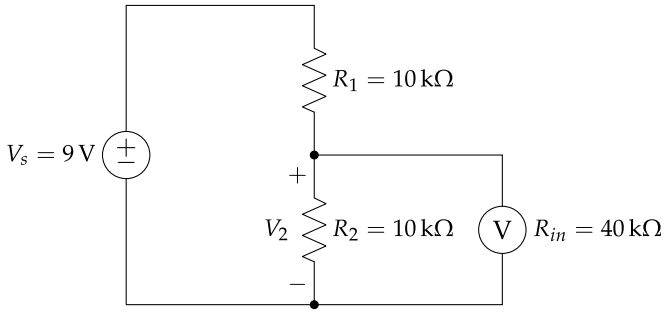
(a) Start at the "+" terminal of the source and follow every connected wire (L5-17 to L5-19). **The circuit has 3 distinct nodes.** Node u_1 joins the "+" terminal of V_s and the left end of R_1. Node u_2 joins the right end of R_1 and the tops of R_2 and R_3. Node u_3 joins all other wires: the "−" terminal of V_s, the bottom of R_2, both ends of R_4, the bottom of R_3 and the long bottom wire. The wire below the right end of R_4 runs down to the bottom wire, and the bottom wire runs back to the "−" terminal of V_s.

(b) **R_4 carries no current.** Both of its ends are on node u_3, so the voltage across it is 0 V, and Ohm's law gives $I = 0\text{ V} / R_4 = 0$. R_4 is shorted, so you can remove it (L6-8).

(c) R_2 and R_3 both connect u_2 to u_3, so they are in parallel: $R_2 \parallel R_3 = (6 \times 3)/(6 + 3)\ \text{k}\Omega = 2\ \text{k}\Omega$. R_1 is in series with this pair: **$R_{eq} = 2\ \text{k}\Omega + 2\ \text{k}\Omega = 4\ \text{k}\Omega$**, and **$I = 12\text{ V} / 4\ \text{k}\Omega = 3\text{ mA}$**. Current divider (L5-14): the current in R_3 is $I \cdot R_2/(R_2 + R_3) = 3\text{ mA} \times 6/(6 + 3) =$ **2 mA**. Check: the pair has 3 mA × 2 kΩ = 6 V across it, and 6 V / 3 kΩ = 2 mA. R_2 carries the other 1 mA.

Problem 3 CIRCUITS EASY 6 POINTS

A 9 V source drives R_1 and R_2 in series. A voltmeter measures V_2, the voltage across R_2. The real meter is an ideal meter in parallel with an input resistance $R_{in} = 40\ k\Omega$.



(a) Find V_2 if the meter is ideal ($R_{in} \to \infty$). (2 points)

(b) Find the voltage that the real meter reads. (2 points)

(c) Find the loading error in percent. State whether a meter with $R_{in} = 1\ M\Omega$ gives a larger or a smaller error. (2 points)

SOLUTION

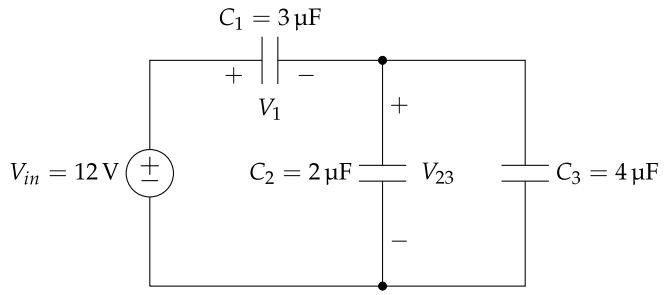
(a) An ideal voltmeter draws no current, so R_1 and R_2 form a voltage divider (L5-12): **$V_2 = 9\ V \times 10/(10 + 10) = 4.5\ V$**.

(b) The real meter puts R_{in} in parallel with R_2 (L5-15): $R_2 \parallel R_{in} = (10 \times 40)/(10 + 40)\ k\Omega = 8\ k\Omega$. The divider now has 10 kΩ above 8 kΩ: **reading = $9\ V \times 8/(10 + 8) = 4.0\ V$**.

(c) **Error = $(4.5\ V - 4.0\ V)/4.5\ V = 1/9 \approx 11\ \%$ (low). The 1 MΩ meter gives a smaller error.** A larger R_{in} draws less current from the divider, so $R_2 \parallel R_{in}$ stays closer to R_2. An ideal voltmeter has $R_{in} \to \infty$ (L5-15). (Check, not required: with $R_{in} = 1\ M\Omega$, R_{in} is 100 times R_2. Then $R_2 \parallel R_{in}$ is only about 1 % below 10 kΩ, and the error falls below 1 %.)

Problem 4 CIRCUITS EASY 7 POINTS

$C_1 = 3\ \mu F$ is in series with the parallel pair $C_2 = 2\ \mu F$ and $C_3 = 4\ \mu F$. The source applies $V_{in} = 12\ V$. All capacitors start uncharged.



(a) Find the equivalent capacitance C_{eq}. (2 points)

(b) Find the charge Q on C_1 and the voltages V_1 and V_{23}. (3 points)

(c) A separate inductor $L = 2\ mH$ carries a current I_L that enters the "+" terminal of V_L. I_L rises at a steady rate from 0 to 6 mA in 3 μs. Find V_L during the rise. (2 points)

SOLUTION

(a) Parallel capacitors add (L6-35): $C_2 + C_3 = 6\ \mu F$. Series capacitors combine like parallel resistors: $\mathbf{C_{eq} = 1/(1/3 + 1/6)\ \mu F = (3 \times 6)/(3 + 6)\ \mu F = 2\ \mu F}$.

(b) $\mathbf{Q = C_{eq} \cdot V_{in} = 2\ \mu F \times 12\ V = 24\ \mu C.}$ C_1 and the pair are in series, so they hold the same charge: the charge that leaves one plate arrives on the next plate. $\mathbf{V_1 = Q/C_1 = 24\ \mu C\ /\ 3\ \mu F = 8\ V}$ and $\mathbf{V_{23} = Q/(C_2 + C_3) = 24\ \mu C\ /\ 6\ \mu F = 4\ V}$. KVL check: 8 V + 4 V = 12 V. The slide formula $V_k = (C_{total}/C_k) \cdot V_{in}$ gives the same $V_1 = (2/3) \times 12\ V = 8\ V$. The smaller capacitance (C_1) takes the larger voltage.

(c) $V_L = L \cdot dI_L/dt$ (L6-36). The current rises at $dI_L/dt = 6\ mA\ /\ 3\ \mu s = 2000\ A/s$. So $\mathbf{V_L = 2 \times 10^{-3}\ H \times 2000\ A/s = 4\ V}$, with "+" at the terminal where I_L enters. V_L stays at 4 V for the whole rise, because the slope is constant.

Problem 5 DEVICES EASY 6 POINTS

A Si sample is doped with phosphorus, $N_D = 10^{16}\ cm^{-3}$. Use $\mu_n = 1250\ cm^2/V \cdot s$.

(a) State whether phosphorus is a donor or an acceptor in Si. State whether the sample is n-type or p-type. Name the majority carrier. (1 point)

(b) Find n and p. (2 points)

(c) Find the conductivity σ and the resistivity ρ. Ignore the holes. (2 points)

(d) The sample is a bar with a length of 0.5 cm and a cross-section area of $2.5 \times 10^{-3}\ cm^2$. Find its resistance R. (1 point)

SOLUTION

(a) Phosphorus is in group V. It has 5 valence electrons: 4 go into bonds, and the fifth is free (L9-13). So phosphorus is a **donor**, the sample is **n-type**, and the **majority carriers are electrons**.

(b) Each donor gives one free electron: $\mathbf{n \approx N_D = 10^{16}\ cm^{-3}}$. From $n \cdot p = n_i^2$: $\mathbf{p = 10^{20}/10^{16} = 10^4\ cm^{-3}}$ (L9-18 to L9-20).

(c) $\mathbf{\sigma = q \cdot \mu_n \cdot n = 1.6 \times 10^{-19} \times 1250 \times 10^{16}\ S/cm = 2.0\ S/cm}$ (because $1.6 \times 1250 = 1.6 \times 1000 + 1.6 \times 250 = 1600 + 400 = 2000$). $\mathbf{\rho = 1/\sigma = 0.5\ \Omega \cdot cm.}$ p is 10^{12} times smaller than n, so the hole term $q \cdot \mu_p \cdot p$ is negligible.

(d) $\mathbf{R = \rho L/A = 0.5\ \Omega \cdot cm \times 0.5\ cm\ /\ (2.5 \times 10^{-3}\ cm^2) = 100\ \Omega}$ (L9-4).

Problem 6 DEVICES EASY 6 POINTS

A red laser emits light at $\lambda = 620$ nm. A near-infrared laser emits light at $\lambda = 1000$ nm.

(a) Find the photon energy of each laser in eV. (2 points)

(b) For each laser, state which of Ge, Si, GaAs and GaP absorb its light. (2 points)

(c) Use the band model (E_c, E_v and E_g) to explain why GaAs is transparent to the 1000 nm light. (2 points)

SOLUTION

(a) **Red: E = 1240/620 = 2.0 eV. Near-infrared: E = 1240/1000 = 1.24 eV.**

(b) A material absorbs a photon only if the photon energy is at least E_g (L9-16). **Red light (2.0 eV): Ge (0.67 eV), Si (1.12 eV) and GaAs (1.42 eV) absorb it; GaP (2.25 eV) does not. Near-infrared light (1.24 eV): Ge and Si absorb it; GaAs and GaP do not.**

(c) In the band model, E_c is the bottom of the conduction band, E_v is the top of the valence band, and $E_g = E_c - E_v = 1.42$ eV for GaAs (L9-15). To absorb a photon, an electron must move from the

valence band (at or below E_v) to the conduction band (at or above E_c). This needs at least E_g = 1.42 eV. The gap has no allowed states, so the electron cannot stop part of the way. **A 1.24 eV photon cannot lift an electron across the gap, so GaAs does not absorb it, and the light passes through.**

Problem 7 DEVICES EASY 7 POINTS

An NMOS transistor has $\mu_n C_{ox} = 200\ \mu A/V^2$, $W/L = 20$ and $V_T = 0.5$ V. Its source is at 0 V.

(a) Find $k' = \mu_n C_{ox}(W/L)$. (1 point)

(b) $V_{GS} = 0.3$ V and $V_{DS} = 1$ V. Find the region and I_D. (1 point)

(c) $V_{GS} = 1.5$ V and $V_{DS} = 0.5$ V. Find the region and I_D. (3 points)

(d) $V_{GS} = 1.5$ V and $V_{DS} = 2$ V. Find the region and I_D. (2 points)

SOLUTION

(a) **$k' = 200\ \mu A/V^2 \times 20 = 4000\ \mu A/V^2 = 4\ mA/V^2$.**

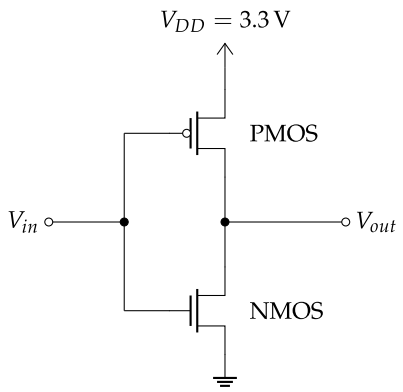
(b) $V_{GS} = 0.3$ V is below $V_T = 0.5$ V, so no channel forms. The transistor is **off**, and **$I_D \approx 0$** (only a small subthreshold leakage, L10-34).

(c) $V_{GS} - V_T = 1.5\ V - 0.5\ V = 1.0$ V. $V_{DS} = 0.5$ V is less than 1.0 V, so the transistor is in the **linear region** (L10-22). $I_D = k' \cdot [(V_{GS} - V_T) \cdot V_{DS} - \tfrac{1}{2} \cdot V_{DS}^2] = 4\ mA/V^2 \times [1.0 \times 0.5 - \tfrac{1}{2} \times 0.5^2]\ V^2 = 4 \times 0.5\ mA - 4 \times 0.125\ mA = 2\ mA - 0.5\ mA =$ **1.5 mA**.

(d) $V_{DS} = 2$ V is at least $V_{GS} - V_T = 1.0$ V, so the transistor is in **saturation**. $I_D = \tfrac{1}{2} \cdot k' \cdot (V_{GS} - V_T)^2 = \tfrac{1}{2} \times 4\ mA/V^2 \times (1.0\ V)^2 =$ **2 mA**.

Problem 8 DEVICES EASY 6 POINTS

A CMOS inverter uses $V_{DD} = 3.3$ V. The NMOS has $V_T = 0.8$ V, and the PMOS has $V_T = -0.8$ V. The NMOS source is at GND, and the PMOS source is at V_{DD}.



(a) Let $V_{in} = 0$ V, and then $V_{in} = 3.3$ V. For each input, find V_{GS} of each transistor. State whether each transistor is on or off. Give V_{out}. (4 points)

(b) The input stays at 0 V or at 3.3 V. Explain why the inverter then draws almost no current from V_{DD}. (2 points)

SOLUTION

(a) For the NMOS, $V_{GS} = V_{in} - 0 = V_{in}$. For the PMOS, $V_{GS} = V_{in} - 3.3$ V. **$V_{in} = 0$ V:** the NMOS has $V_{GS} = 0$ V, which is below 0.8 V, so the **NMOS is off**. The PMOS has $V_{GS} = -3.3$ V, which is below -0.8 V, so the **PMOS is on**. The PMOS connects the output to V_{DD}: **$V_{out} = 3.3$ V** (logic 1). **V_{in}**

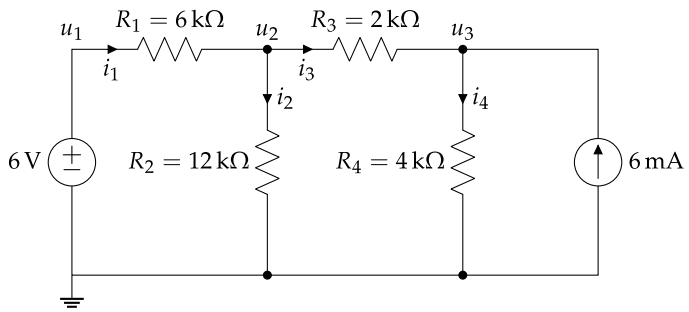
= 3.3 V: the NMOS has $V_{GS} = 3.3$ V, which is above 0.8 V, so the **NMOS is on**. The PMOS has $V_{GS} = 0$ V, which is not below −0.8 V, so the **PMOS is off**. The NMOS connects the output to GND: $\mathbf{V_{out} = 0\ V}$ (logic 0). So input 0 gives output 1, and input 1 gives output 0 (L10-20, L10-25 to L10-28).

(b) In each steady state, one transistor is off. So **no conducting path joins V_{DD} to GND**, and only the small leakage current I_{off} flows (L10-34). The supply delivers a larger current only during a transition, when the PMOS charges the capacitance at the output.

Part II · Long problems (50 points)

Problem 9 CIRCUITS HARD 13 POINTS

Use nodal analysis for this circuit. The bottom node is the reference node (ground). The figure defines the node voltages u_1, u_2 and u_3 and the currents i_1 to i_4.



(a) Which node voltage do you know without a calculation? Give its value and the reason. (1 point)

(b) Write KCL at node u_2 and at node u_3. Use Ohm's law to write each resistor current in terms of the node voltages. (4 points)

(c) Solve for u_2 and u_3. (3 points)

(d) Find i_1 and i_3. Explain the meaning of a negative value. (2 points)

(e) Find the power of the 6 V source and of the 6 mA source. State whether each source absorbs or supplies power. The four resistors absorb 90 mW in total. Show that the powers balance. (3 points)

SOLUTION

(a) The 6 V source connects u_1 to the reference node, so $u_1 - 0 = 6$ V and $\mathbf{u_1 = 6\ V}$ (L6-18). The unknowns are u_2 and u_3.

(b) Work in kΩ, V and mA. Ohm's law gives each current in its arrow direction (L6-20): take the voltage at the arrow tail, subtract the voltage at the arrow head, and divide by R. So $i_1 = (6 - u_2)/6$, $i_2 = u_2/12$, $i_3 = (u_2 - u_3)/2$ and $i_4 = u_3/4$. KCL at u_2 (current in = current out): $i_1 = i_2 + i_3$, so $\mathbf{(6 - u_2)/6 = u_2/12 + (u_2 - u_3)/2}$. Multiply by 12: $12 - 2{\cdot}u_2 = u_2 + 6{\cdot}u_2 - 6{\cdot}u_3$, so $\mathbf{9{\cdot}u_2 - 6{\cdot}u_3 = 12}$. KCL at u_3: the 6 mA source current and i_3 enter, and i_4 leaves, so $6 + i_3 = i_4$ and $\mathbf{6 + (u_2 - u_3)/2 = u_3/4}$. Multiply by 4: $24 + 2{\cdot}u_2 - 2{\cdot}u_3 = u_3$, so $\mathbf{-2{\cdot}u_2 + 3{\cdot}u_3 = 24}$.

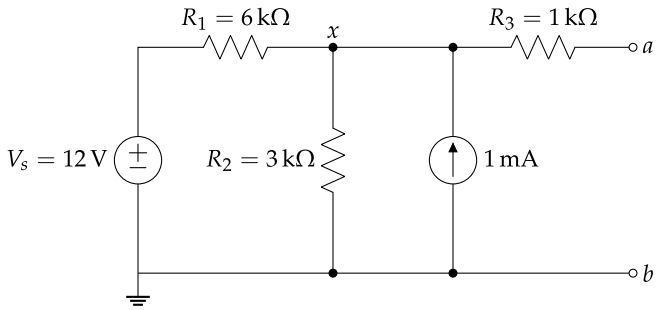
(c) Multiply the second equation by 2: $-4{\cdot}u_2 + 6{\cdot}u_3 = 48$. Add it to the first equation: $5{\cdot}u_2 = 60$, so $\mathbf{u_2 = 12\ V}$. Then $3{\cdot}u_3 = 24 + 2 \times 12 = 48$, so $\mathbf{u_3 = 16\ V}$. (Check: the first equation divided by 3 is $3{\cdot}u_2 - 2{\cdot}u_3 = 4$, and $36 - 32 = 4$.)

(d) $\mathbf{i_1 = (6 - 12)/6 = -1\ mA}$ and $\mathbf{i_3 = (12 - 16)/2 = -2\ mA}$. A negative value means that the current flows opposite to its arrow. So 1 mA flows from u_2 to u_1 through R_1, and 2 mA flows from u_3 to u_2 through R_3. (Not asked: $i_2 = 12/12 = 1$ mA and $i_4 = 16/4 = 4$ mA. KCL check at u_3: 6 mA in = 2 mA + 4 mA out.)

(e) In R_1, 1 mA flows from u_2 to u_1. At u_1 this current enters the "+" terminal of the 6 V source, so the **6 V source absorbs 6 V × 1 mA = 6 mW**. The voltage across the 6 mA source is $u_3 - 0 = 16$ V, with "+" at the top. Its current flows up through it and leaves at the "+" end, so the **6 mA source supplies 16 V × 6 mA = 96 mW**. Balance: the resistors absorb 90 mW (given; 6 + 12 + 8 + 64 mW), and 90 mW + 6 mW = 96 mW, which equals the power supplied. A voltage source can absorb power when the rest of the circuit pushes current into its "+" terminal.

Problem 10 CIRCUITS HARD 12 POINTS

The circuit drives the terminals a and b.



(a) Find the Thevenin voltage $V_{TH} = V_{ab}$ with a–b open. (3 points)

(b) Find the Thevenin resistance R_{TH}. Replace the ideal voltage source by a short circuit and the ideal current source by an open circuit. (2 points)

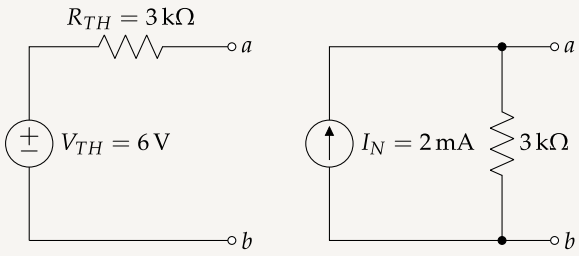
(c) Connect a wire from a to b. Find the Norton current I_N in this wire, and check that $I_N = V_{TH}/R_{TH}$. Then sketch the Thevenin and the Norton equivalent circuits (the sketch is worth 1 of the 3 points). (3 points)

(d) A load $R_L = 3$ kΩ is connected across a–b. Use the Thevenin equivalent to find the load current I and the load voltage V. (2 points)

(e) A capacitor $C = 2$ μF replaces R_L. After a long time, the capacitor voltage no longer changes. Find this voltage and the charge on the capacitor. (2 points)

SOLUTION

The equivalent circuits from (c):



(a) With a–b open, no current flows in R_3, so R_3 has no voltage across it and $V_{ab} = V_x$. KCL at node x (in kΩ, V and mA), with the current in from R_1 and from the source equal to the current out through R_2: $(12 - V_x)/6 + 1 = V_x/3$. Multiply by 6: $12 - V_x + 6 = 2{\cdot}V_x$, so $V_x = 6$ V and $\mathbf{V_{TH} = 6\ V}$.

(b) The shorted voltage source connects the left end of R_1 to the reference node. The opened current source carries no current. From a–b you then see R_3 in series with $R_1 \parallel R_2$: $\mathbf{R_{TH} = 1\ k\Omega + (6 \times 3)/(6 + 3)\ k\Omega = 1\ k\Omega + 2\ k\Omega = 3\ k\Omega}$ (L6-32).

(c) The wire from a to b puts R_3 between x and the reference node. KCL at x: $(12 - V_x)/6 + 1 = V_x/3 + V_x/1$. Multiply by 6: $18 - V_x = 2{\cdot}V_x + 6{\cdot}V_x$, so $V_x = 2$ V. The current in R_3 and in the wire is $\mathbf{I_N = 2\ V\ /\ 1\ k\Omega = 2\ mA}$. Check: $V_{TH}/R_{TH} = 6\ V\ /\ 3\ k\Omega = 2$ mA. **Thevenin equivalent: 6 V in series with 3 kΩ. Norton equivalent: 2 mA in parallel with 3 kΩ** (L6-33).

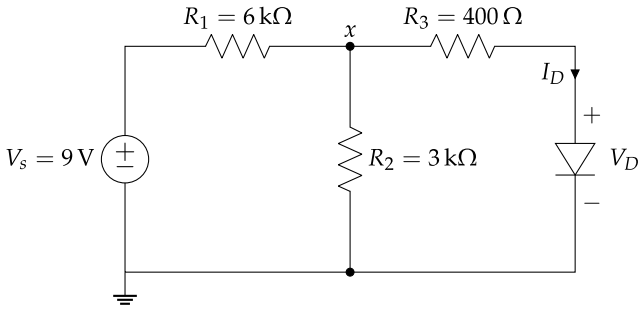
(d) $\mathbf{I = V_{TH}/(R_{TH} + R_L) = 6\ V\ /\ 6\ k\Omega = 1\ mA}$ and $\mathbf{V = I{\cdot}R_L = 1\ mA \times 3\ k\Omega = 3\ V}$. The divider gives the same voltage: $6\ V \times 3/(3 + 3) = 3$ V.

(e) The capacitor voltage is constant, so its current is $i = dQ/dt = C{\cdot}dV/dt = 0$ (from $C = Q/V$, L6-34). With no current, R_{TH} has no voltage across it, so the capacitor sees the open-circuit voltage: $\mathbf{V_C = V_{TH} = 6\ V}$. $\mathbf{Q = C{\cdot}V_C = 2\ \mu F \times 6\ V = 12\ \mu C.}$

Problem 11

DEVICES HARD 13 POINTS

A voltage divider (V_s, R_1 and R_2) drives a Si diode through R_3. The diode has $I_s = 10^{-13}$ A and an ideality factor of 1. I_D is the diode current, and V_D is the diode voltage (anode minus cathode).



(a) Remove the branch with R_3 and the diode. Find the Thevenin equivalent (V_{TH} and R_{TH}) at node x with respect to ground. (3 points)

(b) Put the branch back. Model the conducting diode as a constant 0.6 V drop. Find I_D. (2 points)

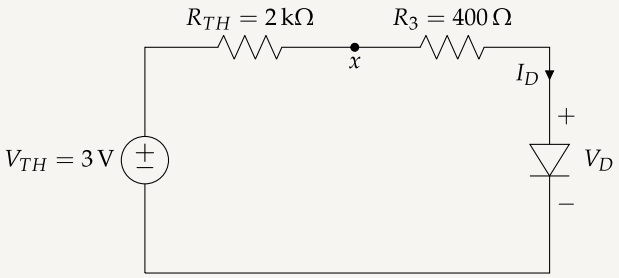
(c) Use the diode equation to find V_D at the current from (b). Use $(kT/q){\cdot}\ln 10 \approx 0.06$ V. Does this V_D agree with the 0.6 V model? (3 points)

(d) Use your results to find V_x and the currents in R_1 and R_2 of the original circuit. (3 points)

(e) The diode is turned around, so its cathode faces node x. Find the diode current and the voltage across the diode. (2 points)

SOLUTION

The Thevenin equivalent from (a) drives the diode branch:



(a) With the branch removed, R_1 and R_2 form a voltage divider: $\mathbf{V_{TH} = 9\ V \times 3/(6 + 3) = 3\ V}$. With the source replaced by a short, R_1 and R_2 are in parallel between x and ground: $\mathbf{R_{TH} = (6 \times 3)/(6 + 3)\ k\Omega = 2\ k\Omega}$ (L6-32).

(**b**) First find the diode state. With no diode current, the anode would be at 3 V and the cathode at 0 V. This is more than 0.6 V, so the diode is forward biased and conducts. KVL around the Thevenin loop: $V_{TH} = I_D \cdot (R_{TH} + R_3) + 0.6$ V. $\mathbf{I_D = (3 - 0.6)\ V\ /\ (2 + 0.4)\ k\Omega = 2.4\ V\ /\ 2.4\ k\Omega = 1\ mA.}$

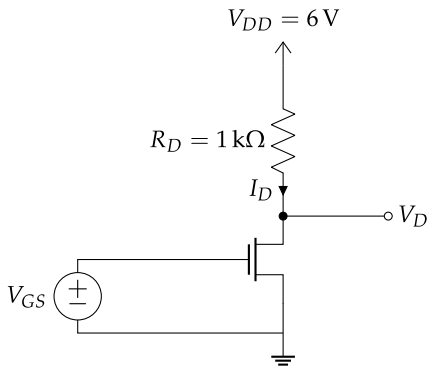
(**c**) I_D is much larger than I_s, so the "−1" term is negligible and $I_D \approx I_s \cdot e^{V_D/(kT/q)}$ (L9-29). Solve for V_D: $V_D = (kT/q) \cdot \ln(I_D/I_s) = (kT/q) \cdot \ln(10^{-3}/10^{-13}) = (kT/q) \cdot \ln(10^{10}) = 10 \times (kT/q) \cdot \ln 10$. Each factor of 10 in the current adds $(kT/q) \cdot \ln 10 \approx 0.06$ V, so $\mathbf{V_D \approx 10 \times 0.06\ V = 0.6\ V}$. **Yes: the 0.6 V model is consistent.** (Not required: the rounding error in 0.06 V per decade is small, so V_D is within a few mV of 0.6 V. A change of a few mV in V_D changes $I_D = (3\ V - V_D)/2.4\ k\Omega$ by less than 1 %, so you do not need a second pass.)

(**d**) In the original circuit, $\mathbf{V_x = V_D + I_D \cdot R_3 = 0.6\ V + 1\ mA \times 0.4\ k\Omega = 1.0\ V}$. The current in R_1, toward x, is $\mathbf{(9 - 1)\ V\ /\ 6\ k\Omega = 4/3\ mA \approx 1.33\ mA}$. The current in R_2, down to ground, is $\mathbf{1\ V\ /\ 3\ k\Omega = 1/3\ mA \approx 0.33\ mA}$. KCL check at x: 4/3 mA in = 1/3 mA + 1 mA out. So the Thevenin equivalent gives the same diode current as the full circuit.

(**e**) The diode is now reverse biased. **Its current is only the reverse saturation current, about $I_s = 10^{-13}$ A, which is practically zero** ($I = I_s \cdot (e^{-3/0.026} - 1) \approx -I_s$, L9-30). With almost no current, R_{TH} and R_3 have no voltage across them. So **the diode has the full 3 V across it, with its cathode 3 V above its anode** (a reverse bias of 3 V).

Problem 12 DEVICES HARD 12 POINTS

An NMOS transistor and a drain resistor $R_D = 1$ kΩ connect to $V_{DD} = 6$ V. The source is at ground, and a voltage source V_{GS} drives the gate. The transistor has $k' = \mu_n C_{ox}(W/L) = 2\ mA/V^2$ and $V_T = 1$ V. It is a long-channel device.



(**a**) Let $V_{GS} = 2$ V. Assume saturation. Find I_D and V_D. Check the assumption. (3 points)

(**b**) For (a), find the gate-to-drain voltage $V_G - V_D$. Compare it with V_T and explain why the channel is pinched off at the drain end. (2 points)

(**c**) Let $V_{GS} = 3$ V. Find I_D and V_D. Show that the transistor is exactly at the edge of saturation. (2 points)

(**d**) Let $V_{GS} = 4$ V. Show that the transistor cannot be in saturation. In the linear region, KVL and the current equation give $V_{DS}^2 - 7 \cdot V_{DS} + 6 = 0$ (V_{DS} in V). Solve this equation, keep the root that meets the region condition, and find I_D. (3 points)

(**e**) Find V_D for $V_{GS} = 0$ V, and compare it with V_D for $V_{GS} = 4$ V. Explain why this circuit acts as an inverter. (2 points)

SOLUTION

(a) $\mathbf{I_D = ½ \cdot k' \cdot (V_{GS} - V_T)^2 = ½ \times 2\ mA/V^2 \times (1\ V)^2 = 1\ mA.}$ KVL from V_{DD} through R_D: $\mathbf{V_D = V_{DD} - I_D \cdot R_D = 6\ V - 1\ mA \times 1\ k\Omega = 5\ V}$. Check: $V_{DS} = 5\ V \geq V_{GS} - V_T = 1\ V$, so the transistor is in saturation, as assumed (L10-22, L10-30).

(b) $\mathbf{V_G - V_D = 2\ V - 5\ V = -3\ V}$, which is below $V_T = 1\ V$. A channel forms only where the gate is more than V_T above the channel, so no channel forms next to the drain: **the channel is pinched off at the drain end** (L10-29, L10-30). The channel ends at the pinch-off point, where the channel voltage reaches $V_{GS} - V_T = 1\ V$. At the source end, $V_G - V_S = 2\ V$ is above V_T, so the channel exists there.

(c) In saturation, $\mathbf{I_D = ½ \times 2\ mA/V^2 \times (3\ V - 1\ V)^2 = 4\ mA}$ and $\mathbf{V_D = 6\ V - 4\ mA \times 1\ k\Omega = 2\ V}$. $V_{DS} = 2\ V = V_{GS} - V_T$, so **the transistor is exactly at the edge of saturation**: $V_G - V_D = 1\ V = V_T$, and the channel charge at the drain end is just zero.

(d) Saturation would give $I_D = ½ \times 2 \times 3^2\ mA = 9\ mA$ and $V_D = 6\ V - 9\ V = -3\ V$. This is impossible, because saturation needs $V_{DS} \geq V_{GS} - V_T = 3\ V$. So the transistor is in the **linear region**. (The given equation comes from KVL, $V_{DS} = 6 - I_D \times 1\ k\Omega$, and the linear-region current $I_D = 2 \cdot [3 \cdot V_{DS} - ½ \cdot V_{DS}^2] = 6 \cdot V_{DS} - V_{DS}^2$, in mA.) Factor: $(V_{DS} - 1) \cdot (V_{DS} - 6) = 0$. The root $V_{DS} = 6\ V$ does not meet the linear-region condition $V_{DS} < 3\ V$, so reject it. $\mathbf{V_D = V_{DS} = 1\ V}$ and $\mathbf{I_D = (6 - 1)\ V\ /\ 1\ k\Omega = 5\ mA}$. Check: $2 \times [3 \times 1 - ½ \times 1^2]\ mA = 5\ mA$.

(e) At $V_{GS} = 0\ V$ the transistor is off ($V_{GS} < V_T$). So $I_D = 0$, R_D has no voltage across it, and $\mathbf{V_D = V_{DD} = 6\ V}$. At $V_{GS} = 4\ V$, $\mathbf{V_D = 1\ V}$. A low input gives a high output, and a high input gives a low output, so **the circuit is an inverter (a NOT gate)**. The transistor acts as a switch to GND (L10-18), and R_D pulls the output up to V_{DD} when the switch is open.